Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1.-6. (canceled)

7. (currently amended) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

pattering a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged in a stagger manner so that side edges of the adjacent hole patterns are only partially opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

8. (original) The method according to claim 7, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

9. (withdrawn) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

pattering a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other, and a distance between the opposing hole patterns is larger at central portions of the respective hole patterns;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

10. (withdrawn) The method according to claim 9, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

11. (withdrawn) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film,

wherein the mask pattern is patterned with a pitch of the hole patterns that makes a distance between opposing central portions of the adjacent storage nodes larger than a distance between opposing corners thereof due to proximity effect during formation of the storage nodes.

12. (withdrawn) The method according to claim 11, wherein the pitch is smaller than 0.55 μm.

13. (withdrawn) The method according to claim 11, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

14. (withdrawn) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

etching an upper potion of the interlayer insulating film between the storage nodes;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

15. (withdrawn) The method according to claim 14, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

16. (new) The method according to claim 7, wherein a relative dielectric constant of the interlayer insulating film is 3.5 or less.

17. (new) The method according to claim 7, wherein the interlayer insulating film is made of silicon oxide including fluorine.

18. (new) The method according to claim 7, wherein the interlayer insulating film is made of SiC.

19. (new) The method according to claim 7, wherein the interlayer insulating film is made of $SiC_xH_yO_z$ ($0<x<1$, $0<y<1$, and $0<z<2$).

20. (new) The method according to claim 7, wherein the interlayer insulating film is made of an amorphous carbon.

21. (new) The method according to claim 7, wherein the length of a portion where the opposing capacitors are overlapped in the mask layout is set so that the value of the parasitic capacitance between adjacent cell capacitors is not more than 10% of the set cell capacitance value.